Amendments to the Drawings

Please replace the originally-filed drawings with 3 replacement sheets that are enclosed.

REMARKS

Claims 2, 4, 6, 14-15, 18, and 20-22 have been cancelled. Claims 1, 3, 8, 12-13, 17, and 19 have been amended. The amendments to claims 3, 8, 12, and 19 serve to cure various typographical errors. Claims 1, 3, 5, 7-13, 16-17, 19, and 23 are currently pending in the application. In view of the following remarks, Applicants respectfully request withdrawal of the rejections and forwarding of the application on to issuance.

The § 102 Rejections

Claims 1, 3, 5, 7-13, 16-17, 19, and 23 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,049,862 to Bauer et al. (hereinafter "Bauer").

Claims 1, 3, 5, 7-13, 16-17, 19, and 23 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,138,229 to Kucukcakar et al. (hereinafter "Kucukcakar").

Claims 1, 3, 5, and 7-12

As amended, claim 1 recites a reconfigurable control structure for CPUs. Specifically, the reconfigurable control structure comprises two control units configured as finite state machines. A multiplexer driven by a selector module is configured to send a single state register a state signal indicating which of the first and second control units generates the control signals for an instruction to be executed.

Bauer does not disclose the claimed subject matter for at least two reasons. First, Bauer does not disclose first and second control units configured as finite state machines. Rather, Bauer simply teaches a decoder device with a programmable decoder section and a hardwired decoder section. There is no indication that Bauer configures either the programmable decoder section or the hardwired decoder section as a finite state machine.

Second, Bauer does not teach a multiplexer driven by a selector module and configured to send a single state register a state signal indicating which of the first and second control units generates the control signals for an instruction to be executed. Rather, Bauer teaches a control unit that detects the category of the compressed program instructions and outputs a control signal to a multiplexer, which selectively connects the programmable decoder

section or the hardwired decoder section to the output of the signal processor. Nowhere does Bauer teach that its control unit or multiplexer is configured to send a state signal to a single state register.

Likewise, Kucukcakar does not disclose the claimed subject matter for at least two reasons. First, Kucukcakar does not disclose first and second control units configured as finite state machines. Rather, Kucukcakar teaches an instruction execution unit that has a non-programmable section and a programmable section that receive an opcode and output control signals for controlling a datapath. There is no indication that Kucukcakar configures either the non-programmable section or the programmable section as a finite state machine.

Second, Kucukcakar does not teach a multiplexer driven by a selector module and configured to send a single state register a state signal indicating which of the first and second control units generates the control signals for the instruction to be executed. In a first embodiment, Kucukcakar teaches that both the non-progammable and programmable sections generate control signals in accordance with decoded opcode signals. Both the non-programmable and programmable sections provide a signal that indicates whether the opcode decoded in the respective section is valid. A selector logic circuit selects either the control signals from the non-programmable section or the programmable section for transfer to the datapath. In a second embodiment, Kucukcakar discloses that the non-programmable section generates control signals in accordance with decoded opcode signals that are transferred through the selector logic circuit to a control bus. A portion of the decoded opcode signals decoded by the non-programmable section generate a start signal that is transmitted to the programming section. The start signal transfers control from the non-programmable section to the programmable section. After the instruction has executed, a signal output from the programmable section causes control for providing the opcode of the next instruction back to the non-programmable section. In neither embodiment does Kucukcakar teach that its control unit is configured to send a state signal to a single state register.

Accordingly, for at least these reasons, this claim is allowable.

Claims 3, 5, and 7-12 depend from claim 1 and, as such, are allowable as depending from an allowable base claim. These claims are also allowable for their recited

features which, in combination with those recited in claim 1, are neither shown nor suggested by the references as cited and applied by the Office.

Claims 13 and 16

As amended, claim 13 recites a process for using a control structure. The process includes executing a function for debugging a first control unit of the control structure and, in the event, in the context of the debugging function, of a given instruction not being implementable in a satisfactory way on the first control unit, implementing the given instruction on a second control unit of the control structure.

Bauer does not disclose the claimed subject matter for at least two reasons. First, Bauer does not disclose executing a function for debugging a first control unit of a control structure. Second, because Bauer does not disclose executing a function for debugging a first control unit, Bauer cannot disclose, in the context of a debugging function, in the event of a given instruction not being implementable in a satisfactory way on the first control unit, implementing the given instruction on a second control unit of the control structure.

Rather, Bauer simply teaches a decoder device with a programmable decoder section and a hardwired decoder section. Bauer teaches that the programmable decoder is used for decoding application-specific program instruction words, which can be changed, while the hardwired decoder section cannot be changed. Nowhere does Bauer teach debugging either the programmable decoder section or the hardwired decoder section. While Bauer discusses purported advantages of utilizing the programmable decoder section, Bauer does not appear to disclose implementing certain program instructions with the programmable decoder section through use of any debugging function.

Likewise, Kucukcakar does not disclose the claimed subject matter for at least two reasons. First, Kucukcakar does not disclose executing a function for debugging a first control unit of a control structure. Second, because Kucukcakar does not disclose executing a function for debugging a first control unit, Kucukcakar cannot disclose, in the context of a debugging function, in the event of a given instruction not being implementable in a satisfactory

way on the first control unit, implementing the given instruction on a second control unit of the control structure.

Rather, Kucukcakar simply teaches an instruction execution unit that has a non-programmable section and a programmable section that receive an opcode and output control signals for controlling a datapath. Nowhere does Kucukcakar discuss debugging either the non-programmable section or the programmable section. Kucukcakar does not disclose implementing certain program instructions with the programmable section through use of any debugging function. On the contrary, Kucukcakar simply teaches that a user can program or reconfigure the programmable section to decode a group of instructions.

Accordingly, for at least these reasons, this claim is allowable.

Claim 16 depends from claim 13 and, as such, is allowable as depending from an allowable base claim. This claim is also allowable for its recited features which, in combination with those recited in claim 13, are neither shown nor suggested by the references as cited and applied by the Office.

Claims 17, 19, and 23

Although the language of claims 17, 19, and 23 is not identical to that of claim 1, the allowability of claims 17, 19, and 23 will be apparent in view of the above discussion of claim 1.

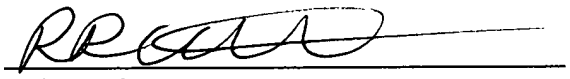
Conclusion

Applicants respectfully submit that all pending claims are in condition for allowance. Accordingly, Applicants request that a Notice of Allowance be issued. If the Office's next anticipated action is to be anything other than a Notice of Allowance, Applicants request that the undersigned be contacted for scheduling a telephone interview.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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